PATENT

Case Docket No. IMEC92.001DV1
Date: April 26, 2004

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s)	:	Brockmeyer, et al.
Appl. No.	:	10/766,159
Filed	:	January 27, 2004
For	:	OPTIMIZED DATA TRANSFER AND STORAGE ARCHITECTURE FOR MPEG-4 MOTION ESTIMATION ON MULTI-MEDIA PROCESSORS
Examiner	:	Unknown
Group Art Unit	:	Unknown

I hereby certify that this correspondence and all marked attachments are being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on

April 26, 2004
(Date)

Eric M. Nelson, Reg. No. 43,829

TRANSMITTAL LETTER

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Enclosed for filing in the above-identified application are:

(X) An Information Disclosure Statement.

(X) A PTO Form 1449 with nineteen (19) references.

(X) The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment, to Account No. 11-1410.

(X) Return prepaid postcard.

Eric M. Nelson
Registration No. 43,829
Attorney of Record
Customer No. 20,995
(619) 235-8550

S:\DOCS\EMN\EMN-4555.DOC:sad
042604

INFORMATION DISCLOSURE STATEMENT

Applicant	:	Brockmeyer, et al.
App. No.	:	10/766,159
Filed	:	January 27, 2004
For	:	OPTIMIZED DATA TRANSFER AND STORAGE ARCHITECTURE FOR MPEG-4 MOTION ESTIMATION ON MULTI-MEDIA PROCESSORS
Examiner	:	Unknown
Group Art Unit	:	Unknown

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Enclosed is form PTO-1449 listing 19 references that are of record in U.S. patent application No. 09/261,804, filed March 3, 1999, now U.S. Patent No. 6,690,835 issued February 10, 2004, which is the parent of this divisional application, and is relied upon for an earlier filing date under 35 U.S.C. § 120. Copies of the references are not submitted pursuant to 37 C.F.R. § 1.98(d).

This Information Disclosure Statement is being filed with an RCE or within three months of the filing date of this application and no fee is required in accordance with 37 C.F.R. § 1.97(b)(1), (b)(2), or (b)(4).

Respectfully submitted,

KNOBBE, MARTENS, OLSON & BEAR, LLP

Dated: 4/26/2004

By: _____

Eric M. Nelson
Registration No. 43,829
Attorney of Record
Customer No. 20,995
(619) 235-8550

S:\DOCS\EMN\EMN-4553.DOC:sad
042604

FORM PTO-1449 U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. IMEC92.001DV1	APPLICATION NO. 10/766,159
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (USE SEVERAL SHEETS IF NECESSARY)	APPLICANT Brockmeyer, et al.	
	FILING DATE January 27, 2004	GROUP Unknown

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (IF APPROPRIATE)
	1.	5,208,673	5/1993	Boyce			
	2.	5,630,033	5/1997	Purcell et al.			
	3.	6,028,631	2/2000	Nakaya et al			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
							YES	NO
	4.	EP0698861A1	02/28/95	Europe				
	5.	EP 0 698 861 A1	02/28/96	Europe				
	6.	EP0848558A1	07/18/97	Europe				
	7.	EP 0 848 558 A1	06/17/98	Europe				

EXAMINER INITIAL		OTHER DOCUMENTS (INCLUDING AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.)
	8.	Diguet, et al., **Formalized methodology for data reuse exploration in hierarchical memory mappings**, *Proceeding 1997 International Symposium on Low Power Electronics and Design, Monterey, CA USA, Aug. 18-20 1997* pp30-35
	9.	Greef, et al., **Mapping real-time motion estimation type algorithms to memory efficient, programmable multi-processor architectures**, *Microprocessing and Microprogramming* 41:409-423 (1995)
	10.	Copy of European Search Report; Application No. EP 99 10 4301.
	11.	Greef, et al., Mapping real-time motion estimation type algorithms to memory efficient, programmable multi-processor architectures, Microprocessing and Microprogramming 41 (1995) 409-423.
	12.	IEEE workshop on VLSI signal processing, La Jolla, CA, Oct, 1994. "Global communication and memory optimizing transformations for low power signal processing systems", Catthoor, et al., 12 pages
	13.	IEEE Journal Of Solid-State Circuits, Vol. 31, No. 9, September 1996. "Energy Dissipation In General Purpose Microprocessors" Gonzalez, et al., pages 1277 - 1283
	14.	Proceedings of the IEEE, Vol. 83, No. 2, February 1995. "VLSI Architectures for Video Compression - A Survey", Pirsch, et al., pages 220 - 246
	15.	IEEE Transactions on Circuits and Systems for Video Technology, Vol. 6, No. 1, February 1996. "Architecture and Applications of the HiPAR Video Signal Processor", Ronner, et al., pages 56 - 66
	16.	IEEE Workshop on VLSI signal processing, Monteray, CA, Oct. 1996. "Low Power Storage Exploration for H.263 Video Decoder", Nachtergaele, et al., 12 pages
	17.	In a paper collection on Low Power CMOS design, IEEE Press, pp. 609-618. "System-level transformation for low power data transfer and storage", Catthoor, et al., pages 1 - 8
	18.	Proc. IEEE Intnl. Symp. on Low Power Design, Monteray, Aug. 1996 "Power Exploration for Data Dominated Video Applications", Wuytack, et al., pages 359 - 364
	19.	IEEE Transactions on Circuits and Systems for Video Technology, Vol. 7, No. 1, February 1997. "The M-PEG Video Standard Verification Model", Thomas Sikora, pages 19 - 31

S:\DOCS\EMN\EMN-4552.DOC:sad
042604

EXAMINER	DATE CONSIDERED

*EXAMINER: INITIAL IF CITATION CONSIDERED, WHETHER OR NOT CITATION IS IN CONFORMANCE WITH MPEP 609; DRAW LINE THROUGH CITATION IF NOT IN CONFORMANCE AND NOT CONSIDERED, INCLUDE COPY OF THIS FORM WITH NEXT COMMUNICATION TO APPLICANT.

X Did not receive any FOR or NPL.